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Shin et al.

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(54) **SEMICONDUCTOR DEVICE WITH BURIED GATE AND METHOD FOR FABRICATING THE SAME**

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H01L 27/108 (2006.01)
H01L 29/423 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 27/10876*** (2013.01); ***H01L 27/10855*** (2013.01); ***H01L 27/10888*** (2013.01); ***H01L 29/4236*** (2013.01)

(58) **Field of Classification Search**
CPC H01L 27/10876; H01L 27/10855; H01L 27/10888; H01L 29/4236
See application file for complete search history.

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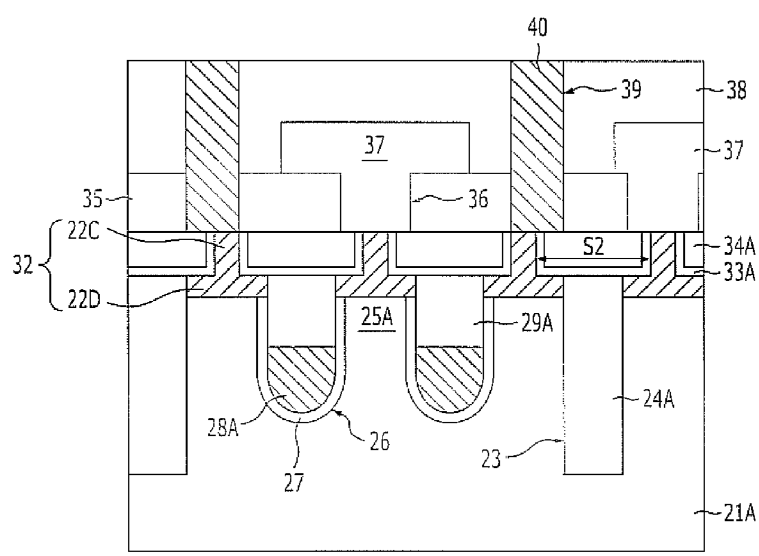
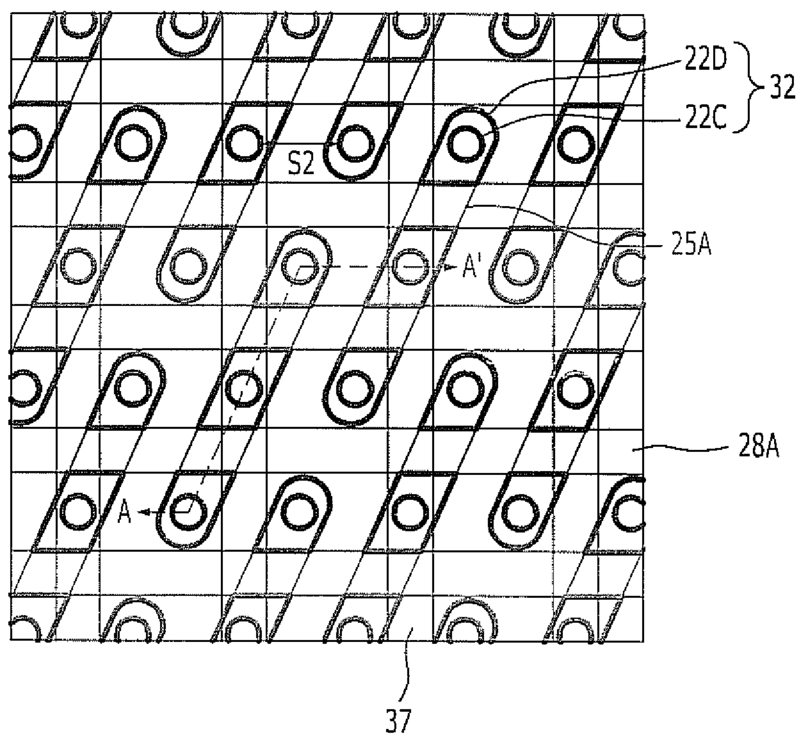
(57) **ABSTRACT**

A method for fabricating a semiconductor device includes forming landing plugs over a substrate, forming a trench by etching the substrate between the landing plugs, forming a buried gate to partially fill the trench, forming a gap-fill layer to gap-fill an upper side of the buried gate, forming protruding portions of the landing plugs, and trimming the protruding portions of the landing plugs.

5 Claims, 9 Drawing Sheets

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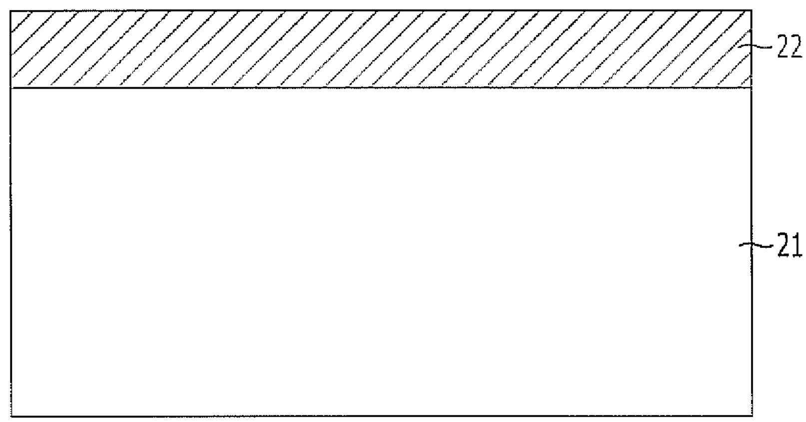
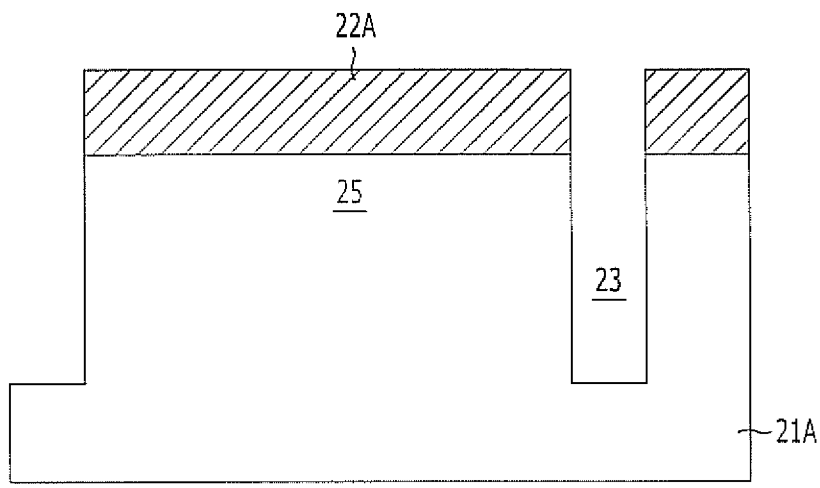


FIG. 2B



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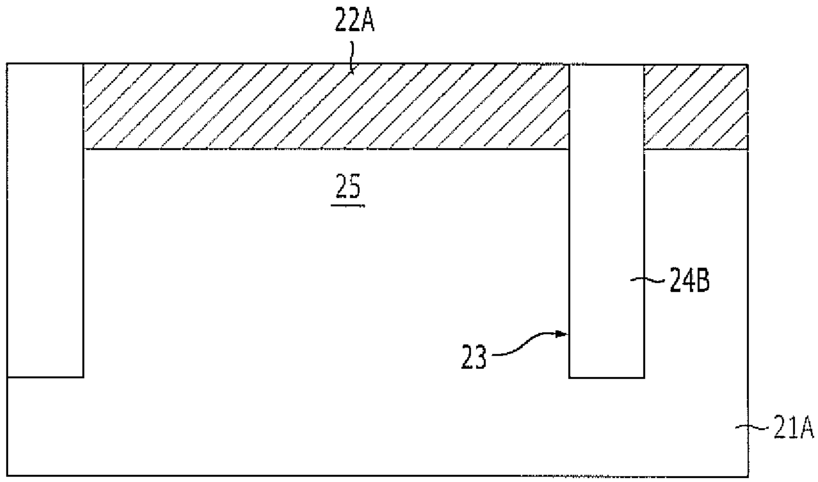


FIG. 2D

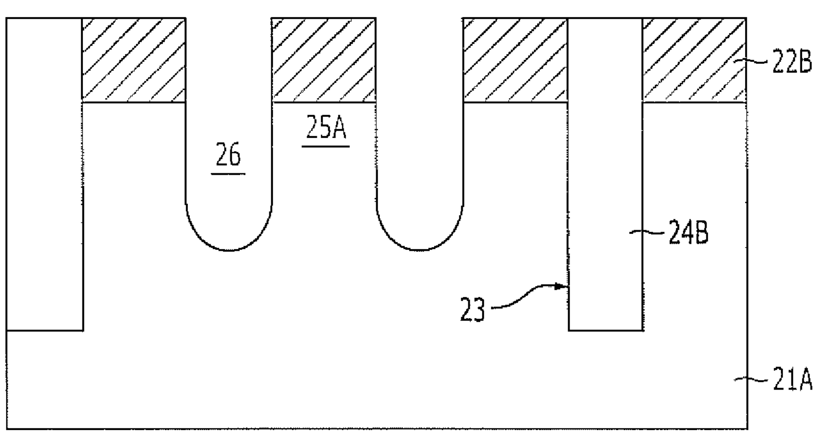
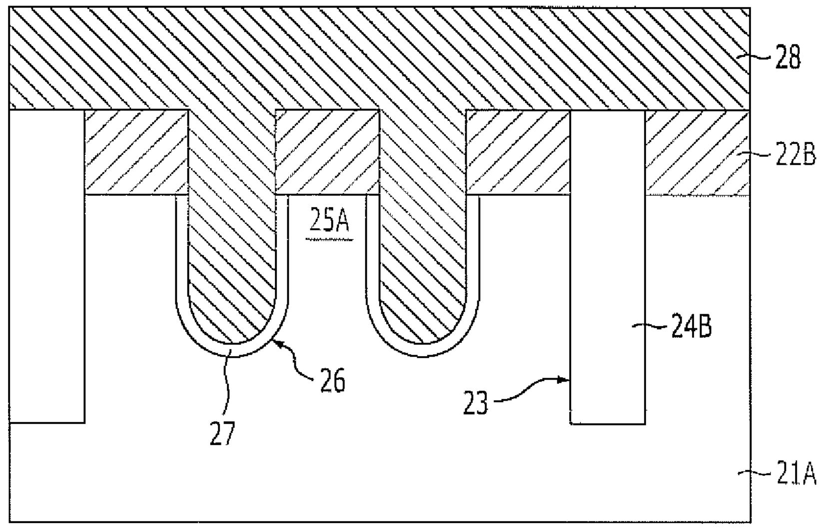


FIG. 2E



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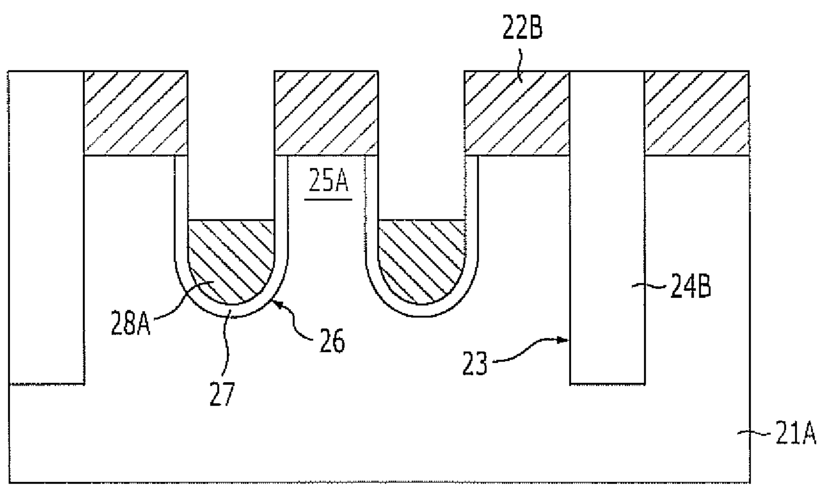

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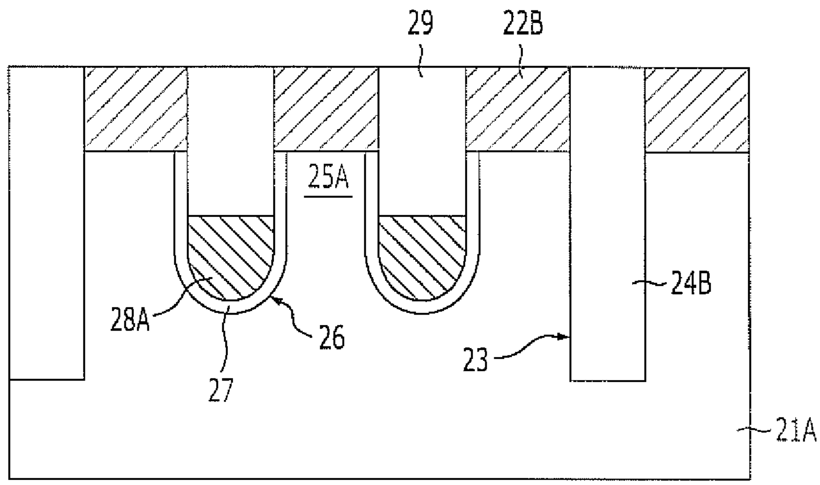


FIG. 2H

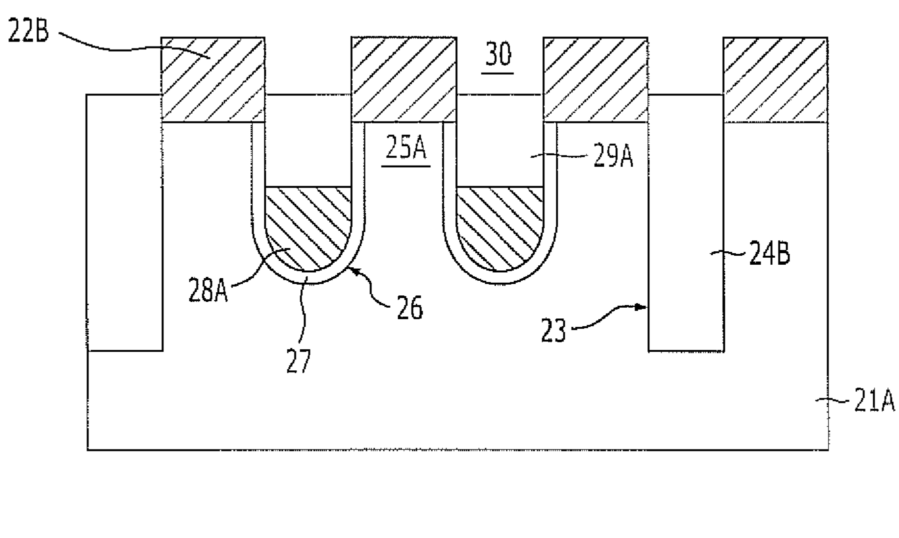
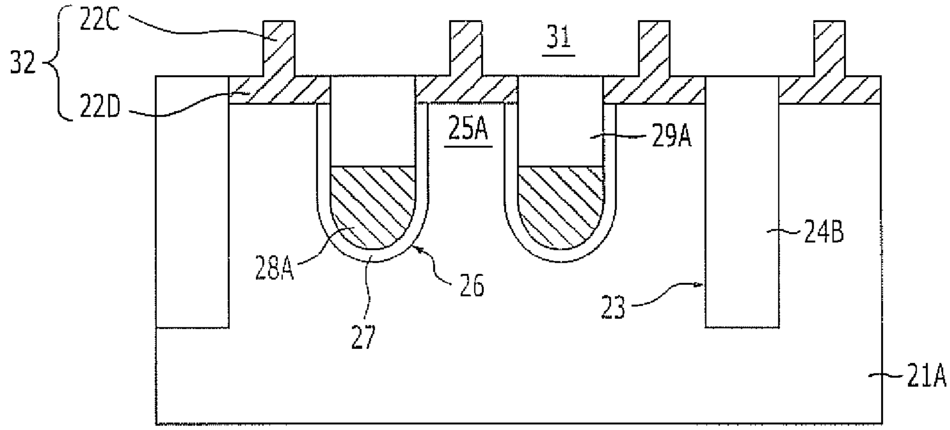


FIG. 2I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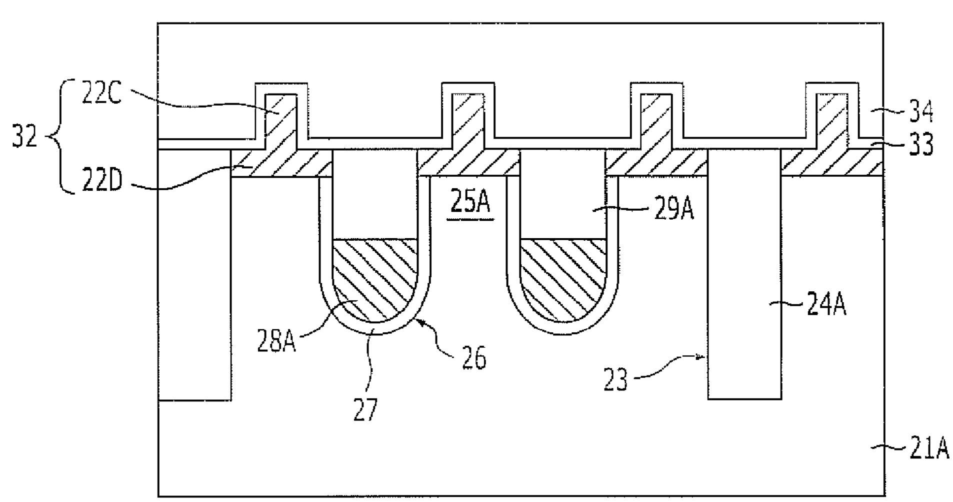
32
22D
31
25A
29A
24B
28A
26
27
23
21A

FIG. 2J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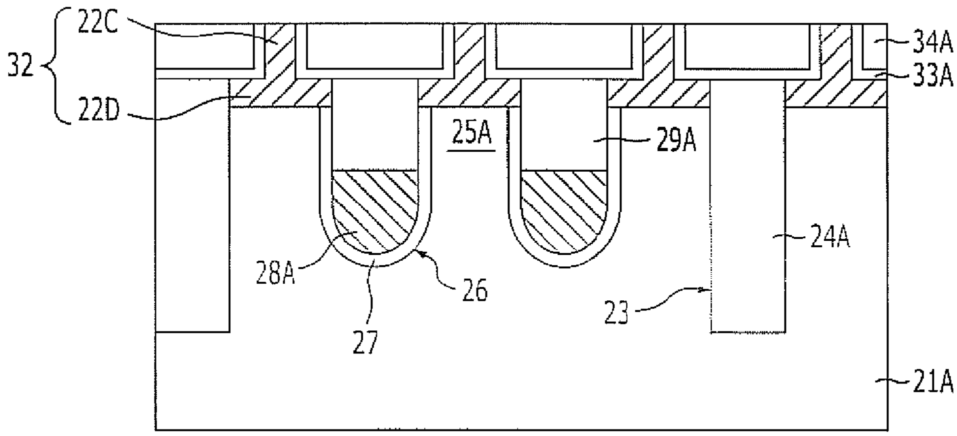
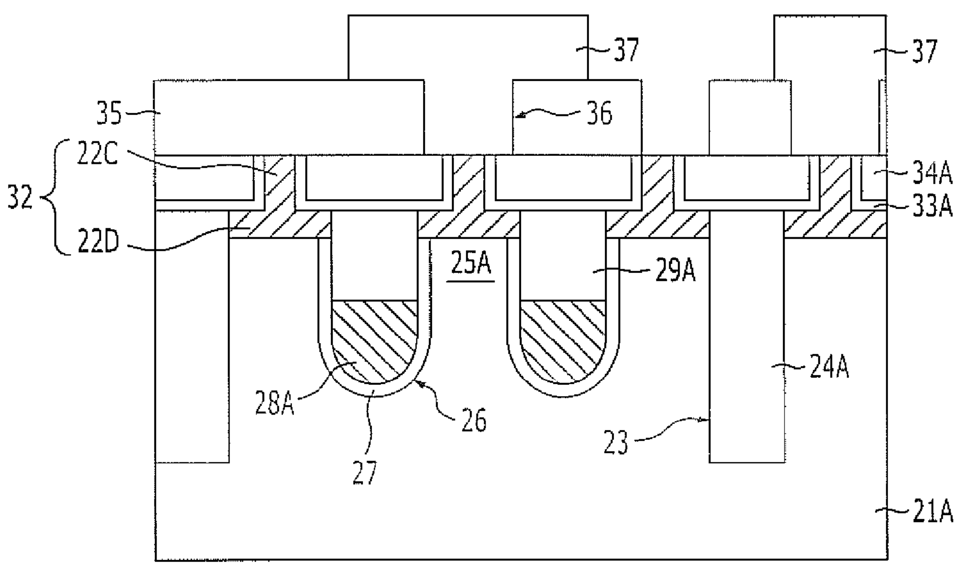
33
25A
29A
24A
28A
26
27
23
21A

FIG. 2K



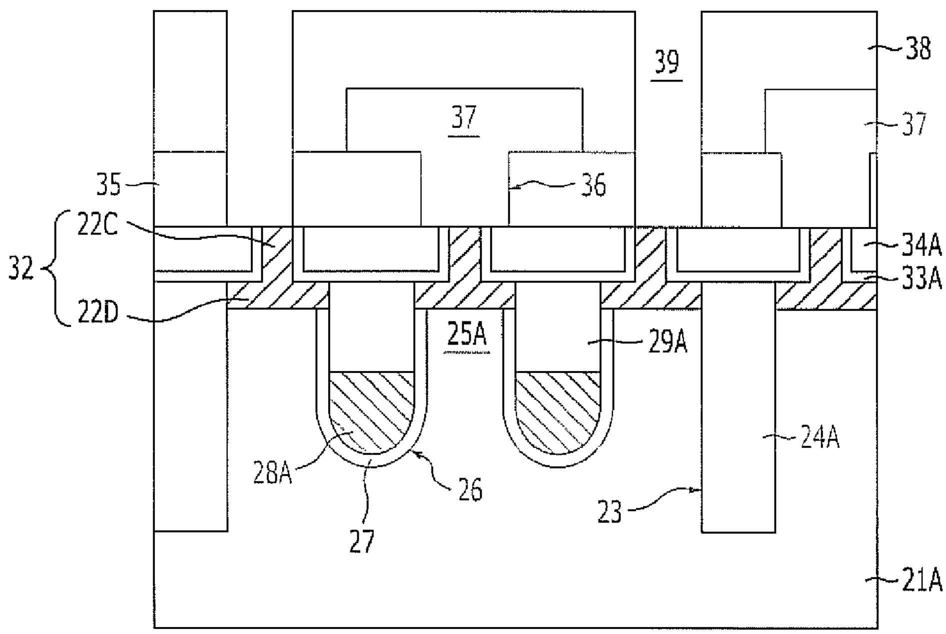
22C
32
22D
34A
33A
25A
29A
24A
28A
26
27
23
21A

FIG. 2L



37
37
35
36
22C
32
22D
34A
33A
25A
29A
24A
28A
26
27
23
21A

FIG. 2M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37
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35
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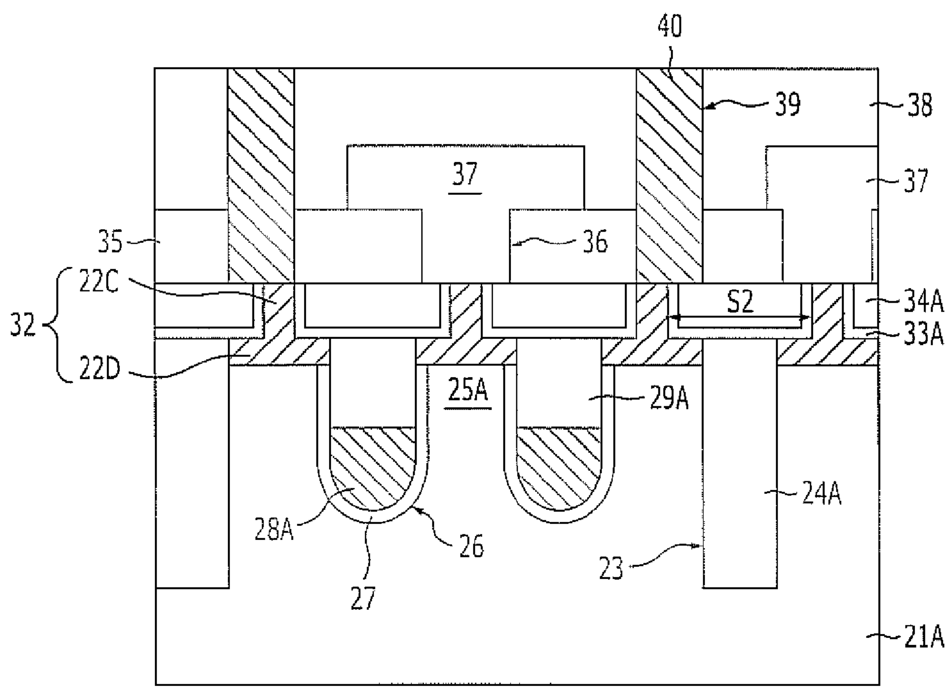
22D
25A
29A
24A
28A
26
23
27
21A

FIG. 2N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35
36
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32
33A
22D
25A
29A
24A
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26
23
27
21A

FIG. 3A

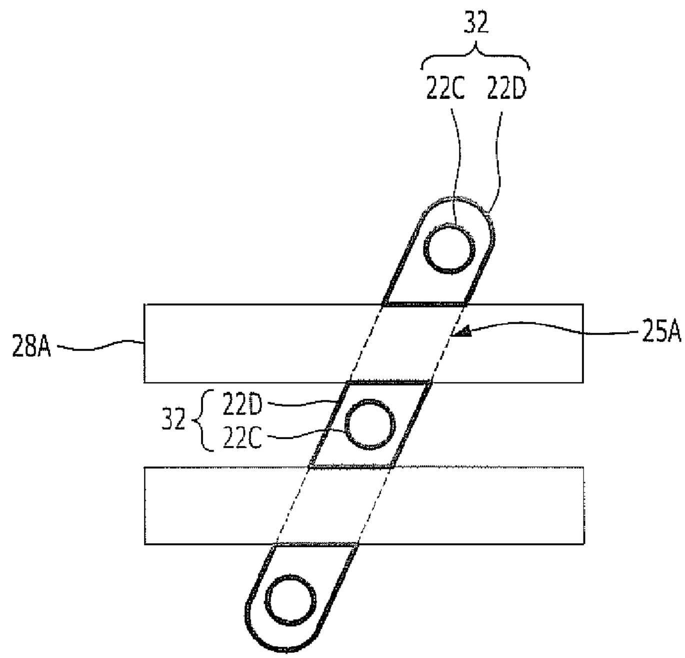
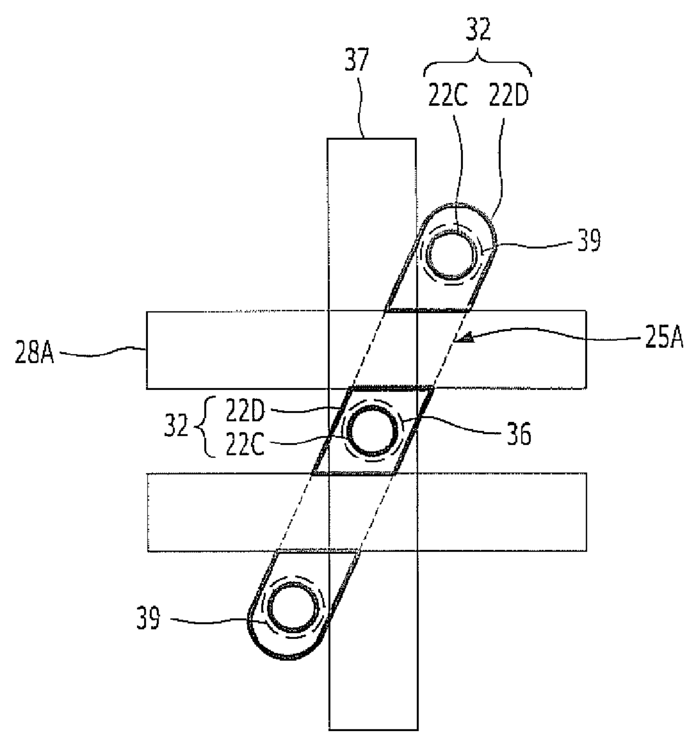

32
22C
22D
28A
25A
32
22D
22C

FIG. 3B


32
37
22C
22D
39
28A
25A
32
22D
22C
36
39

SEMICONDUCTOR DEVICE WITH BURIED GATE AND METHOD FOR FABRICATING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

This application is a division of U.S. patent application Ser. No. 12/827,385 filed on Jun. 30, 2010, now U.S. Pat. No. 8,247,324 which claims priority of Korean Patent Application No. 10-2009-0134849 filed on Dec. 30, 2009. The disclosure of each of the foregoing applications is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

Exemplary embodiments of the present invention relate to a method for fabricating a semiconductor device, and more particularly, to a semiconductor device with a buried gate and a method for fabricating the same.

In a sub 60-nanometer (nm) DRAM process, it may be advantageous to form a buried gate in order to increase the integration degree of transistors in a cell, simplify the process, and improve device characteristics such as a leakage characteristic.

A method for fabricating the buried gate is performed by forming a trench and burying a gate in the trench. Therefore, the interference between a bit line and the gate may be minimized, and the number of films to be stacked may be reduced. Furthermore, the capacitance of the cells may be reduced to thereby improve a refresh characteristic.

In general, after a buried gate is formed in a cell region, a sealing process may be performed for sealing the upper side of the buried gate using a gap-fill layer. A gate oxidation process and a gate conductive layer formation process may be performed to form a transistor of a peripheral circuit region by exposing only the peripheral circuit region. A contact etching process and a bit-line (BL) process may be performed to form a bit-line contact hole by exposing the cell region.

In this method, however, since a storage node contact hole is formed after the bit line is formed in the cell region, it is difficult to obtain an exposed contact area for forming the storage node contact hole. Furthermore, since the exposed contact area is narrow, interfacial resistance between a storage node contact and a substrate may increase.

In particular, when the process is performed on the basis of a design rule of $6F^2$, an active region in which a bit-line contact hole is to be formed should ideally be completely covered by the bit line. Therefore, when the area of the bit line is increased, an exposed contact margin for forming the storage node contact hole is further decreased.

To increase the process margin of the storage node contact hole, the storage node contact hole and the storage node contact may be formed before the bit line is formed. In order to prevent a bridge between the bit line and the storage node contact, the bit line should ideally be formed as large as possible. In this case, however, the area of the storage node contact is reduced to cause an increase in contact resistance.

SUMMARY OF THE INVENTION

Exemplary embodiments of the present invention are directed to a semiconductor device which may prevent a bridge between a storage node contact and a bit line and a method for fabricating the same.

In accordance with an exemplary embodiment of the present invention, a method for fabricating a semiconductor device includes forming landing plugs over a substrate, forming a trench by etching the substrate between the landing plugs, forming a buried gate to partially fill the trench, forming a gap-fill layer to gap-fill an upper side of the buried gate, forming protruding portions of the landing plugs, and trimming the protruding portions of the landing plugs.

In accordance with another exemplary embodiment of the present invention, a method for fabricating a semiconductor device includes forming landing plugs over a substrate, forming a trench by etching the substrate between the landing plugs, forming a buried gate to partially fill the trench, forming a first gap-fill layer to gap-fill an upper side of the buried gate, forming protruding portions of the landing plugs, trimming the protruding portions of the landing plugs, forming a spacer dielectric layer over the entire surface including the trimmed landing plugs, forming a second gap-fill layer over the spacer dielectric layer, and planarizing the second gap-fill layer and the spacer dielectric layer to expose surfaces of the trimmed landing plugs.

In accordance with yet another exemplary embodiment of the present invention, a semiconductor device includes a substrate having a trench arranged therein, a buried gate partially filling the trench, gap-fill layers arranged over the buried gate and protruding from a surface of the substrate, and a landing plug having a buried portion arranged over the substrate between gap-fill layers and a protruding portion arranged on the buried portion.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a plan view of a semiconductor device in accordance with an exemplary embodiment of the present invention.

FIGS. **2**A to **2**N are cross-sectional views illustrating a method for fabricating a semiconductor device in accordance with another exemplary embodiment of the present invention.

FIG. **3**A is a plan view of a buried gate and a landing plug.

FIG. **3**B is a plan view of the buried gate and the landing plug including a bit line.

DESCRIPTION OF EXEMPLARY EMBODIMENTS

Exemplary embodiments of the present invention will be described below in more detail with reference to the accompanying drawings. The present invention may, however, be embodied in different forms and should not be construed as being limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the present invention to those skilled in the art. Throughout the disclosure, like reference numerals refer to like parts throughout the various figures and embodiments of the present invention.

The drawings are not necessarily to scale and in some instances, proportions may have been exaggerated in order to clearly illustrate features of the embodiments. When a first layer is referred to as being "on" a second layer or "on" a substrate, it not only refers to a case where the first layer is formed directly on the second layer or the substrate but also a case where a third layer exists between the first layer and the second layer or the substrate.

FIG. **1** is a plan view of a semiconductor device in accordance with an exemplary embodiment of the present invention.

Referring to FIG. **1**, a buried gate **28**A may be formed in an active region **25**A. Landing plugs **32** may be formed on the active region **25**A. Each of the landing plugs **32** has a buried portion **22**D and a protruding portion **22**C. The landing plugs **32** may be formed on the active region **25**A between the buried gates **28**A. The landing plugs **32** may include a landing plug in which a bit line contact is to be formed and a landing plug in which a storage node contact is to be formed. A bit line **37** may be formed in a direction crossing the buried gate **28**A.

Referring to FIG. **1**, the protruding portion **22**C has a smaller area than the buried portion **22**D. Accordingly, a space S**2** between the protruding portions **22**C is relatively large.

As described above, since the space S**2** between the protruding portions **22**C is large, it is possible to minimize a bridge between a bit line contact hole and a storage node contact hole. Accordingly, the process margin of the bit line contact hole and storage node contact hole process may be improved.

FIGS. **2**A to **2**N are cross-sectional views illustrating a method for fabricating a semiconductor device in accordance with another exemplary embodiment of the present invention, taken along a line A-A' of FIG. **1**.

Referring to FIG. **2**A, a first conductive layer **22** may be formed on a substrate **21**. The first conductive layer **22** may formed to a thickness of 100 Å to 500 Å. The first conductive layer **22** may include polysilicon.

Referring to FIG. **2**B, a shallow trench isolation (STI) process may be performed for device isolation. In the STI process, a first conductive pattern **22**A may be formed by etching the first conductive layer **22** using a photoresist pattern (not illustrated). The substrate **21** may then be etched by using the first conductive pattern **22**A as an etching barrier. Accordingly, a first trench **23** having a constant depth may be formed in the substrate **21**A. The first trench **23** defines an active region **25**.

Referring to FIG. **2**C, a dielectric layer, such as a spin-on dielectric (SOD), may be formed to gap-fill the first trench **23**. A planarization process, such as a chemical mechanical polishing (CMP) process, may then be performed to form a device isolation layer **24** which gap-fills the first trench **23**.

Referring to FIG. **2**D, a mask and etching process for a buried gate process may then be performed. A plurality of landing plugs **22**B may be formed by etching the first conductive pattern **22**A using a photoresist pattern (not illustrated), for example. The substrate **21** between the respective landing plugs **22**B may then be etched. Accordingly, second trenches **26** having a predetermined depth may be formed in the substrate **21**A. The second trenches **26** may be formed by etching the active region **25** and the device isolation layer **24** at the same time. After the second trenches **26** are formed, the active region is represented by reference numeral **25**A. Before the photoresist pattern is formed, a buried gate hard mask layer may be formed on the entire surface including the landing plugs **22**B. The buried gate hard mask layer may include a nitride layer. The buried gate hard mask layer may be used as an etching barrier for forming the second trenches **26**.

The landing plugs **22**B may be formed so as to be aligned with the device isolation layer **24**. This is referred to as a self-aligned landing plug process. When the self-aligned landing plug process is performed, the height of the landing plugs **22**B may be 400 Å or more.

Referring to FIG. **2**E, a gate insulation layer **27** may then be formed on the surfaces of the second trenches **26**.

A second conductive layer **28** may then be formed on the entire surface including the gate insulation layer **27** so as to gap-fill the second trenches **26**. The second conductive layer **28** may include a titanium nitride layer (TiN), a tantalum nitride layer (TaN), or a tungsten layer (W).

Referring to FIG. **2**F, the second conductive layer **28** may then be planarized by a CMP process or the like such that the surfaces of the landing plugs **22**B are exposed. An etch back process may then be performed to form buried gates **28**A to partially fill the second trenches **26**.

Referring to FIG. **2**G, a first gap-fill layer **29** may then be formed to gap-fill the upper side of the buried gates **28**A. The first gap-fill layer **29** may include an oxide layer, a nitride layer, or a multilayered structure consisting of an oxide layer and a nitride layer. For example, a nitride layer may be thinly applied, and an oxide layer, such as SOD, may be formed to gap-fill the upper side of the buried gates **28**A.

The first gap-fill layer **29** may then be planarized to expose the surfaces of the landing plugs **22**B.

Referring to FIG. **2**H, the first gap-fill layer **29** and the device isolation layer **24** may then be recessed to a predetermined depth. Accordingly, a first recess **30** may be formed between the respective landing plugs **22**B. A first gap-fill layer **29**A and a device isolation layer **24**A remain after the first recesses **30** are formed. The landing plugs **22**B may partially protrude from the first recesses **30**. For example, the landing plugs **22**B may protrude from the first recesses **30** by 200 Å or more.

Referring to FIG. **2**I, a trimming process may then be performed. The trimming process selectively removes portions of the protruding part of the landing plugs **22**B. Accordingly, the landing plugs **22**B are formed into landing plugs **32**. The trimming process may remove the side portions of the landing plug **22**B by 10 Å or more. Each of the landing plugs **32** formed by the trimming process may include a protruding portion **22**C and a buried portion **22**D. A second recess **31** may then be formed between the respective protruding portions **22**C. An isotropic etching process may be used for forming the landing plugs **32**. The protruding portion **22**C has a structure that may be etched in a side direction by the isotropic etching process. The buried portion **22**D has a structure that is buried between the first gap-fill layers **29**A. The top surface area of each landing plug **32** is reduced to the protruding portion **22**C. Since the buried portion **22**D maintains the first area, the contact area between the buried portion **22**D and the substrate **21**A may be maintained.

In accordance with the above-described exemplary embodiment, the protruding portion **22**C and the buried portion **22**D of each landing plug **32** may have different areas. Since the area of the buried portion **22**D contacting the active region **25**A is relatively large, it is possible to constantly maintain the contact resistance with the active region **25**A. On the other hand, since the protruding portion **22**C has a relatively small area, the protruding portion **22**C may increase an open area between the landing plug **32** and a bit line contact hole or a storage node contact hole which is to be formed in a subsequent process.

The landing plugs **32** include a landing plug to be connected to a bit line contact and a landing plug to be connected to a storage node contact. Therefore, the landing plug **32** to be connected to a bit line contact may be formed in the center of the active region **25**A, and the landing plug **32** to be connected to a storage node contact may be formed on both sides of the center of the active region **25**A. Accordingly, the landing plug **32** to be connected to a bit line contact may have the same shape as the landing plug **32** to be connected to a storage node contact.

Referring to FIG. **2**J, a spacer dielectric layer **33** may then be formed on the entire surface including the landing plugs **32**, and a second gap-fill layer **34** may then be formed on the spacer dielectric layer **33** so as to gap-fill the space between the landing plugs **32**. The spacer dielectric layer **33** may include a nitride layer. The spacer dielectric layer **33** may be formed to a thickness of 100 Å or more. The second gap-fill layer **34** may include an oxide layer, such as SOD.

Referring to FIG. **2**K, a planarization process may then be performed until the surfaces of the protruding portions of the landing plugs **32** are exposed. During the planarization process, the second gap-fill layer **34** and the spacer dielectric layer **33** may also be planarized. Accordingly, the spacer **33**A and the second gap-fill layer **34**A remain between the landing plugs **32**. The spacer **33**A serves to prevent a bridge between contacts during a subsequent bit line contact process or storage node contact process. Furthermore, the spacer **33**A prevents the landing plugs **32** from being damaged by a subsequent process.

Referring to FIG. **2**L, a first interlayer dielectric layer **35** may then be formed on the entire surface. Before the first interlayer dielectric layer **35** is formed, an etching stop layer may be formed. The etching stop layer may then be formed to a thickness of 100 Å or more by using a nitride layer, for example.

The first interlayer dielectric layer **35** may then be etched to form a bit line contact hole exposing one of the landing plugs **32**. A bit line **37** may then be formed to be connected to the exposed landing plug **32** through the bit line contact hole **36**. The exposed landing plug **32** corresponds to a landing plug formed in the center of the active region **25**A between the buried gates **28**A, as seen in FIG. **2**L. The bit line **37** may be formed in a direction crossing the buried gate **28**A. A portion of the bit line **37**, which is buried in the bit line contact hole **36**, becomes a bit line contact.

Referring to FIG. **2**M, a second interlayer dielectric layer **38** may then be formed on the entire surface including the bit line **37**, and a storage node contact hole **39** may then be formed to expose one of the landing plugs **32**. The exposed landing plug **32** corresponds to a landing plug formed on both sides of the center of the active region **25**A, as seen in FIG. **2**M.

Referring to FIG. **2**N, a storage node contact **40** may then be formed to fill the storage node contact hole **39**.

Since the space S2 between the landing plugs **32** may be increased by the protruding portions **22**C, a process margin for preventing a bridge between the bit line **37** and the storage node contact **40** may be improved.

The semiconductor device having the storage node contact **40** formed therein includes the substrate **21**A having the trenches **26** formed therein, the buried gates **28**A partially filling the trenches **26**, the first gap-fill layers **29**A which may be formed on the buried gates **28**A so as to protrude from the surface of the substrate **21**A, and the landing plugs **32** each having the buried portion **22**D formed on the substrate **21**A between the first gap-fill layers **29**A and the protruding portion **22**C formed on the buried portion **22**D. The protruding portion **22**C may have a smaller area than the buried portion **22**D. The landing plug **32** may include a polysilicon layer. The semiconductor device may include the bit line contact or the storage node contact **40** formed on the landing plug **32**. The bit line contact is a portion of the bit line **37** which is buried in the bit line contact hole **36**.

FIG. **3**A is a plan view of the buried gate and the landing plug. FIG. **3**B is a plan view of the buried gate and the landing plug including the bit line.

Referring to FIGS. **3**A and **3**B, the buried gate **28**A may be formed in the active region **25**A, and the landing plugs **32** may be formed on the active region **25**A. The landing plugs **32** do not overlap the buried gate **28**A. Each of the landing plugs **32** has the protruding portion **22**C and the buried portion **22**D. The bit line **37** may cross the buried gate **28**A at right angles. A portion of the bit line **37** may be buried in the bit line contact hole **36** and connected to one of the landing plugs **32**, and the storage node contact holes **39** may be formed over the other landing plugs **32**.

In accordance with the above-described exemplary embodiment of the present invention, the landing plugs **32** having the protruding portions **22** with a small area may be formed by the trimming process. Therefore, the bridge between the bit line contact hole **36** and the storage node contact hole **39** may be minimized. Accordingly, the process margin of the bit line contact hole **36** and the storage node contact hole **39** may be improved. Furthermore, since the landing plugs **32** having the protruding portions **22**C with a relatively small area are formed, the open area between the bit line contact hole **36** and the landing plug **32** or the open area between the storage node contact hole **39** and the landing plug **32** may be increased.

Furthermore, the storage node contact hole **39** and the storage node contact **40** are formed after the bit line **37** is formed. The bit line **37** and the storage node contact **40** are all formed in the cell region.

In accordance with another exemplary embodiment of the present invention, a gate of a peripheral circuit region may be formed at the same time that a bit line is formed.

In accordance with still another exemplary embodiment of the present invention, an interlayer dielectric layer may be formed after a gate of a peripheral circuit region is formed. Then, a storage node contact may be formed, and a bit line may be formed by a Damascene process.

When the bit line contact hole or the storage node contact hole is formed, the process may be stopped by the etching stop layer, and an additional etching process may be performed to form the contact hole. The additional etching process promotes the etching of the nitride layer. Accordingly, the nitride layer used as the spacer **33**A may be partially removed to increase the open area between the bit line contact hole and the landing plug or the open area between the storage node contact hole and the landing plug. Furthermore, a loss of the active region may be prevented.

In the above-described embodiment of the present invention, the landing plugs **22**B are first formed, and the buried gates **28**A are then formed. Accordingly, the open margins of the bit line contact hole **36** and the storage node contact hole **39** may be improved, and the contact resistance to the active region **25**A may be reduced.

In accordance with the exemplary embodiments of the present invention, since the landing plugs having the protruding portions with a small area and the buried portions with a large area may be formed by the trimming process, it may be possible to prevent a bridge between the bit line contact hole and the storage node contact hole. Accordingly, the process margin of the bit line contact hole and storage node contact hole process may be improved. Furthermore, since the contact area between the landing plug and the active region may be increased by the buried portion having a large area, it may be possible to uniformly maintain contact resistance.

While the present invention has been described with respect to the specific embodiments, it will be apparent to those skilled in the art that various changes and modifications may be made without departing from the spirit and scope of the invention as defined by the following claims.

What is claimed is:

1. A semiconductor device comprising:

a substrate having a trench arranged therein;

a buried gate partially filling the trench;

a first gap-fill layer arranged over the buried gate and protruding from a surface of the substrate; a landing plug having a buried portion arranged over the substrate between the first gap-fill layer and a protruding portion arranged over the buried portion;

a second gap-fill layer formed over the first gap-fill layer; and

a spacer formed between the first gap-fill layer and the second gap-fill layer and surrounding sidewalls and a bottom surface of the second gap-fill layer,

wherein an upper surface of the buried gate is lower than a bottom surface of the landing plug, and

wherein the protruding portion of the landing plug has a smaller area than the buried portion of the landing plug.

2. The semiconductor device of claim **1**, wherein the landing plug comprises a polysilicon layer.

3. The semiconductor device of claim **1**, further comprising a contact arranged on the landing plug.

4. The semiconductor device of claim **3**, wherein the contact comprises a bit line contact and a storage node contact.

5. The semiconductor device of claim **1**,

wherein the spacer is formed of different material from the second gap-fill layer.

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